AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit comprising a first filter and a first mixer configured to generate an upconverted signal in response to mixing an input signal and a first oscillation signal, wherein said first filter is implemented at a quality factor which allows (i) said first filter to filter undesired channels from said upconverted signal and (ii) said first mixer to be integrated on the same integrated circuit as said first filter;

a second circuit comprising a second filter and a second mixer configured to generate a downconverted signal in response to mixing said upconverted signal and a second oscillation signal, wherein said second filter is implemented at a quality factor which allows (i) said second filter to filter undesired channels from said downconverted signal and (ii) said second mixer to be integrated on the same integrated circuit as said second filter; and

a third circuit configured to generate an output signal in response to mixing said downconverted signal ~~and~~ with a third oscillation signal ~~derived from said second oscillation signal~~, wherein (i) said third oscillation signal is generated by dividing said second oscillation signal in said second circuit and (ii) said

third circuit is configured to filter undesired channels from said output signal.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein (i) said first circuit comprises~~:~~ a low noise amplifier configured to receive said input signal~~,~~, (ii) said ~~a~~ first mixer is coupled to an output of said low noise amplifier~~,~~ and (iii) said ~~a~~ first filter is coupled to an output of said first mixer and configured to generate said upconverted signal.

3. (ORIGINAL) The apparatus according to claim 2, wherein said first filter comprises an intermediate frequency filter and is further configured to receive said first oscillation signal.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein:

said second circuit further comprises~~: a second mixer pair configured to receive said upconverted signal,~~ a first summation circuit configured to receive one or more outputs of said second mixer ~~pair~~; and

said ~~a~~ second filter is configured to receive an output of said summation circuit and generate said downconverted signal.

5. (CURRENTLY AMENDED) The apparatus according to claim 4, wherein said second mixer ~~pair~~ is configured to receive an in phase signal of said second oscillation signal and a quadrature phase signal of said second oscillation signal, wherein said second filter comprises an intermediate frequency filter.

6. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said third circuit comprises:

a third mixer ~~pair~~ configured to receive said downconverted signal;

a second summation circuit configured to receive one of the outputs of said third mixer ~~pair~~; and

a third filter configured to (i) receive an output of said summation circuit and (ii) generate said output signal.

7. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said third mixer ~~pair~~ is configured to receive an in phase signal of said third oscillation signal and a quadrature signal of said third oscillation signal, wherein said third filter comprises a SAW filter.

8. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is further configured to provide selectivity and gain while not degrading a quality of the input signal.

9. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to reduce unwanted noise or distortion.

10. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises a single microchip architecture.

11. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is implemented on a plurality of microchips.

12. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises a tuner.

13. (ORIGINAL) The apparatus according to claim 6, wherein said third mixer comprises an image reject type mixer.

14. (CURRENTLY AMENDED) An apparatus comprising:

means for generating an upconverted signal with a first filter and a first mixer in response to an input signal and a first oscillation signal, wherein said first filter is implemented at a quality factor which allows (i) said first filter to filter undesired channels from said upconverted signal and (ii) said first mixer to be integrated on the same integrated circuit with said first filter;

means for generating a downconverted signal with a second filter and a second mixer in response to mixing said upconverted signal and a second oscillation signal, wherein said second filter is implemented at a quality factor which allows (i) said second filter to filter undesired channels from said downconverted signal and (ii) said second mixer to be integrated on the same integrated circuit with said second filter; and

means for generating an output signal in response to mixing said downconverted signal ~~and~~ with a third oscillation signal ~~derived from said second oscillation signal~~, wherein (i) said third oscillation signal is generated by dividing said second oscillation signal in said means for generating said downconverted signal and (ii) said means for generating said output signal is configured to filter undesired channels from said output signal.

15. (CURRENTLY AMENDED) A method for filtering undesired channels from an output signal, comprising the steps of:

(A) generating a upconverted signal with a first filter and a first mixer in response to an input signal and a first oscillation signal, wherein said first filter is implemented at a quality factor which allows (i) said first filter to filter undesired channels from said upconverted signal and (ii) said first mixer to be integrated on the same integrated circuit as said first filter;

(B) generating a downconverted signal with a second filter and a second mixer in response to an upconverted signal and a second oscillation signal, wherein said second filter is implemented at a quality factor which allows (i) said second filter to filter undesired channels from said downconverted signal and (ii) said second mixer to be integrated on the same integrated circuit as said second filter; and

(C) generating said output signal in response to said downconverted signal ~~and~~ with a third oscillation signal ~~derived from said second oscillation signal~~ wherein said third oscillation signal is generated by dividing said second oscillation signal.

16. (CURRENTLY AMENDED) The method according to claim 15, wherein step (A) comprises:

receiving said input signal by a low noise amplifier;

coupling ~~a~~ said first mixer to an output of said low noise amplifier; and

coupling ~~a~~ said first filter to an output of said first mixer to generate said upconverted signal.

17. (ORIGINAL) The method according to claim 16, wherein said first filter comprises an intermediate frequency filter and said first mixer is further configured to receive said first oscillation signal.

18. (CURRENTLY AMENDED) The method according to claim 15, wherein step (B) comprises:

receiving said upconverted signal by ~~a~~ said second ~~mixer pair~~ mixer;

configuring a first summation circuit to receive one or more outputs of said second mixer ~~pair~~; and

configuring a second filter to receive an output of said summation circuit to generate said downconverted signal.

19. (CURRENTLY AMENDED) The method according to claim 15, wherein step (C) comprises:

configuring a third mixer ~~pair~~ to receive said downconverted signal;

configuring a second summation circuit to receive one outputs of said third mixer ~~pair~~; and

configuring a third filter to receive an output of said summation circuit to generate said output signal.

20. (CURRENTLY AMENDED) The method according to claim 18, wherein said second mixer ~~pair~~ is configured to receive an in phase signal of said second oscillation signal and a quadrature phase signal of said second oscillation signal.

21. (ORIGINAL) The method according to claim 15, wherein said method is implemented on a single microchip architecture.

22. (ORIGINAL) The method according to claim 15, wherein said method is implemented on a plurality of microchips.

23. (CURRENTLY AMENDED) The method according to claim 19, wherein said third mixer ~~pair~~ is configured to receive an in phase signal of said third oscillation signal and a quadrature phase signal of said third oscillation signal in quadrature phase.